Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **OUTPUT A**
2. **INPUT A –**
3. **INPUT A +**
4. **V –**
5. **INPUT B +**
6. **INPUT B –**
7. **OUTPUT B**
8. **V +**

**2 1 8 7 6**

**3 4 5**

**DIE ID**

**L**

**F**

**4**

**4**

**2**

**B**

**.050”**

**.101”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential: V-**

**Mask Ref: LF442B**

**APPROVED BY: DK DIE SIZE .050” X .101” DATE: 12/7/18**

**MFG: NATIONAL SEMI THICKNESS .015” P/N: LF442**

**DG 10.1.2**

#### Rev B, 7/19/02